μPD41254*
65,536 x 4-BIT DYNAMIC NMOS RAM

Description

The NEC μPD41254* is a 65,536-word by 4-bit dynamic N-channel MOS random-access memory (RAM) designed to operate from a single +5V power supply. The negative voltage substrate bias is generated internally providing automatic and transparent operation.

The μPD41254* utilizes double polylayer N-channel silicon gate processing which provides for high storage cell density, high performance, and high reliability.

The device also utilizes a single transistor dynamic storage cell and advanced dynamic circuitry throughout, including the 1024 sense amplifiers, which ensures that power dissipation is minimized.

The three-state I/O is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the I/O by holding $\overline{CAS}$ low. The data I/O then is returned to the high impedance state by returning $\overline{CAS}$ to the high state. The μPD41254* hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

Refresh is accomplished by utilizing a $\overline{CAS}$ before $\overline{RAS}$ cycle that will enable the internal generation of the refresh address. Refresh can also be accomplished using $\overline{RAS}$-only refresh as a normal read or write cycle on the 256 address combinations of A_0–A_7, during a 4ms period.

Features

- ☐ 65,536-word x 4-bit organization
- ☐ Standard 18-pin DIP
- ☐ $\overline{CAS}$ before $\overline{RAS}$ internal address refresh mode
- ☐ Multiplexed address inputs
- ☐ Single +5V ± 10% power supply
- ☐ On-chip substrate bias generator
- ☐ Low power dissipation: 28mw (standby max)
  413mw (active, t_{RC} = 270ns)
- ☐ Nonlatched I/O, TTL-compatible
- ☐ All inputs TTL-compatible, and low input capacitance
- ☐ 256-cycle, 4ms refresh (A_0–A_7 pins for refresh address)
- ☐ 2 performance ranges:

Device	Access Time	R/W Cycle	RMW Cycle
μPD41254-15*	150ns	270ns	355ns
μPD41254-20*	200ns	335ns	445ns

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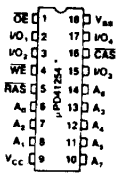
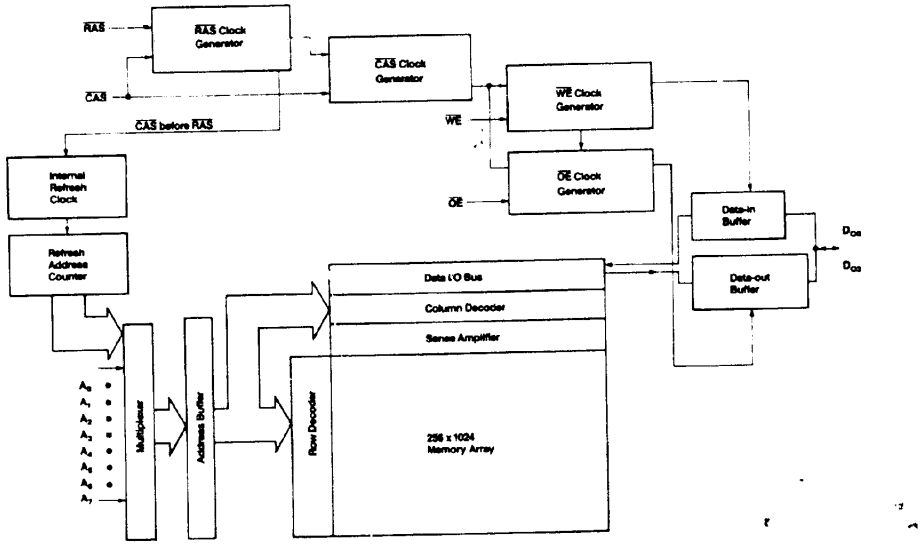
Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	$\overline{OE}$	Output Enable
2, 3, 15, 17	I/O_1–I/O_4	Data Input/output
4	$\overline{WE}$	Write Enable
5	$\overline{RAS}$	Row Address Strobe
6–8, 10–14	A_0–A_7	Address Inputs
9	V_{CC}	+5V Power Supply
16	$\overline{CAS}$	Column Address Strobe
18	V_{SS}	Ground

Block Diagram



Absolute Maximum Ratings*

Voltage On Any Pin Relative to V_{SS}	−1.0V to +7.0V
Operating Temperature, T_A (Ambient)	0°C to +70°C
Storage Temperature, T_{STG} (Ambient)	−55°C to +150°C
Short-circuit Output Current	50mA
Power Dissipation, P_D	1w

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Power Supply Standby Current	I_{CC2}			5	mA	$\overline{RAS}$ = V_{IH}, D_{OUT} = high impedance
I/O Leakage Current	$I_{I(L)}$	−10		10	μA	Any input V_{IN} = 0V to V_{CC}, all other pins not under test = 0V
Output Leakage Current	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ 5.5V
Output High (Logic 1) Voltage	V_{OH}	2.4			V	I_{OUT} = −2mA
Output Low (Logic 0) Voltage	V_{OL}			0.4	V	I_{OUT} = 4.2mA
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input High (Logic 1) Voltage, All Inputs	V_{IH}	2.4		5.5	V	
Input Low (Logic 0) Voltage, All Inputs	V_{IL}	1.0		0.8	V	

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AC Characteristics ① ② ③

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 10% ④

Parameter	Symbol	Limits 41254-15* Min	41254-15* Max	41254-20* Min	41254-20* Max	Unit	Test Conditions
Average power supply operating current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = $t_{RC(MIN)}$)	I_{CC1}		75		65	mA	⑤
Average power supply current, refresh mode ($\overline{RAS}$, cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = $t_{RC(MIN)}$)	I_{CC3}		65		60	mA	⑤
Average power supply current, page mode operation ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = $t_{PC(MIN)}$)	I_{CC4}		45		40	mA	⑤
Random read or write cycle time	t_{RC}	270		335		ns	⑨
Read-write cycle time	t_{RWC}	355		445		ns	⑥
Page mode cycle time	t_{PC}	170		225		ns	⑥
Access time from $\overline{RAS}$	t_{RAC}		150		200	ns	⑦ ⑧
Access time from $\overline{CAS}$	t_{CAC}		75		100	ns	⑦ ⑧
Output buffer turn-off delay	t_{OFF}	0	40	0	50	ns	⑩
Transition time (rise and fall)	t_T	3	35	3	50	ns	④
$\overline{RAS}$ precharge time	t_{RP}	100		120		ns	
$\overline{RAS}$ pulse width	t_{RAS}	150	10,000	200	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	75		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	75	10,000	100	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	150		200		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	30	75	35	100	ns	⑪
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0		0		ns	⑫
$\overline{CAS}$ precharge time, nonpage cycles	t_{CPN}	25		30		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	60		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		ns	
ROW address set-up time	t_{ASR}	0		0		ns	
ROW address hold time	t_{RAH}	20		25		ns	
Column address set-up time	t_{ASC}	0		0		ns	
Column address hold time	t_{CAH}	45		55		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	120		155		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	20		25		ns	⑬
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	⑬
Write command hold time	t_{WCH}	45		55		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	120		155		ns	
Write command pulse width	t_{WP}	45		55		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	45		55		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	45		55		ns	
Data-in set-up time	t_{DS}	0		0		ns	⑭
Data-in hold time	t_{DH}	45		55		ns	⑭
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	120		155		ns	
Refresh period	t_{REF}		4		4	ms	

AC Characteristics (Cont.)

Parameter	Symbol	Limits 41254-15* Min	41254-15* Max	41254-20* Min	41254-20* Max	Unit	Test Conditions
$\overline{WE}$ command set-up time	t_{WCS}	0		0		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	120		155		ns	
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	195		255		ns	
Access time from $\overline{OE}$	t_{OEA}		40		50	ns	
Data delay time	t_{OED}	40		50		ns	
Output turn-off delay to $\overline{OE}$	t_{OEZ}	0	40	0	50	ns	
$\overline{OE}$ command hold time	t_{OEH}	0		0		ns	
Average power supply current, $\overline{CAS}$ before $\overline{RAS}$ refresh mode ($\overline{RAS}$, cycling, $\overline{CAS}$ = V_{IL}; t_{RC} = $t_{RC(MIN)}$	I_{CC5}		65		60	mA	⑤
$\overline{CAS}$ set-up time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CSR}	10		10		ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	t_{CHR}	30		35		ns	

Notes:
① An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved
② AC measurements assume t_T = 5ns
③ V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}
④ All voltages referenced to V_{SS}
⑤ I_{CC1}, I_{CC3} and I_{CC4} depend on output loading and cycle rates. Specified values are obtained with the output open
⑥ The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C to +70°C) is assured
⑦ Load = 2 TTL loads and 100pF
⑧ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown
⑨ Assumes that $t_{RCD} \geq t_{RCD}$ (max)
⑩ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}
⑪ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}
⑫ t_{CRP} requirement should be applicable for $\overline{RAS}$ $\overline{CAS}$ cycles preceded by any cycle
⑬ Either t_{RRH} or t_{RCH} must be satisfied for a read cycle
⑭ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles

Capacitance

T_A = 0°C to +70°C; V_{CC} = +5.0V ± 10%

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance, Address Inputs	C_{I1}			5	pF	
Input Capacitance, Strobe Inputs	C_{I2}			8	pF	
Input/Output Capacitance, Data Ports	$C_{I/O}$			7	pF	

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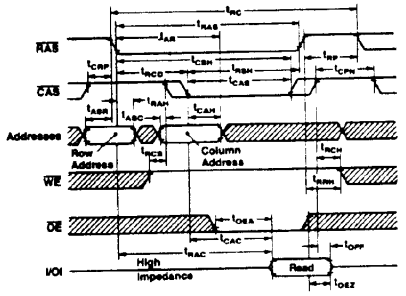
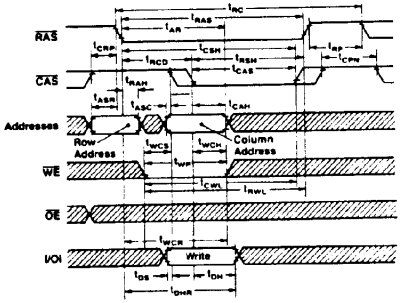
Timing Waveforms

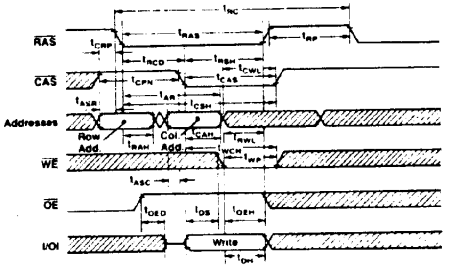
Read Cycle



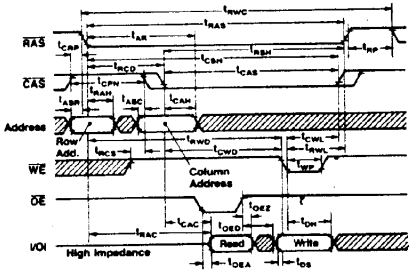
Write Cycle (Early Write)



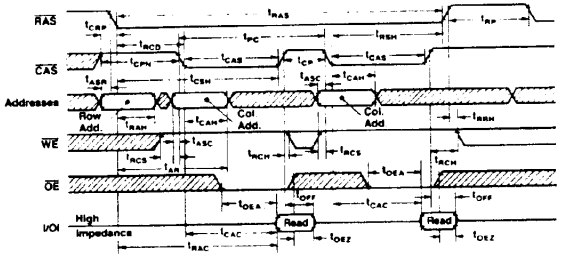
Write Cycle (OE Controlled)



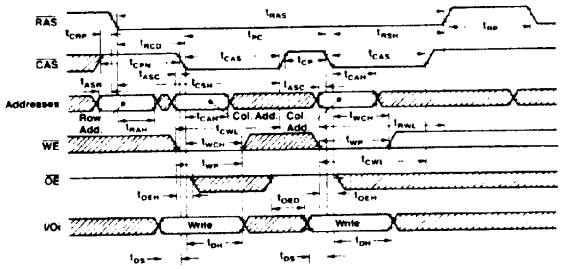
Read-write/Read-modify-write Cycles



Page Mode Read Cycle



Page Mode Write Cycle



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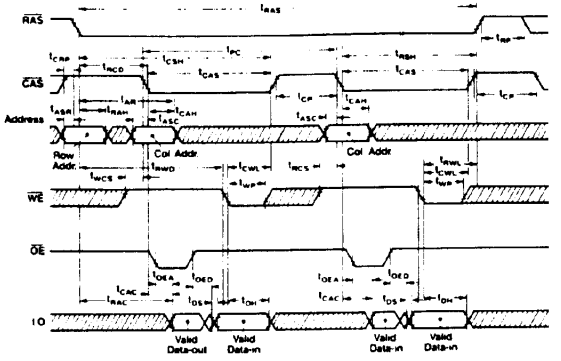
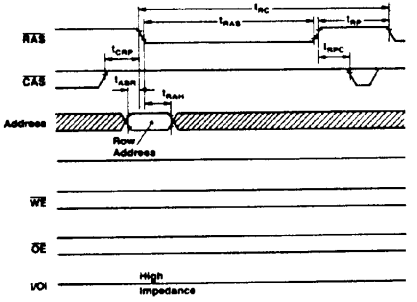
Timing Waveforms (Cont.)

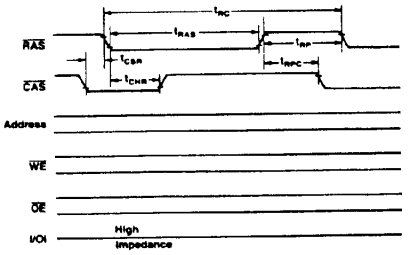
Page Mode Read-Write/Read-Modify-Write Cycles



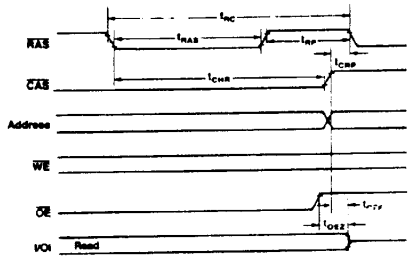
RAS-only Refresh Cycle



CAS Before RAS Refresh Cycle



Hidden Refresh Cycle



Package Outlines

For information, see Section 9.

Plastic, μPD41254C*
Ceramic, μPD41254D*

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41254DS-5-84-CAT-L